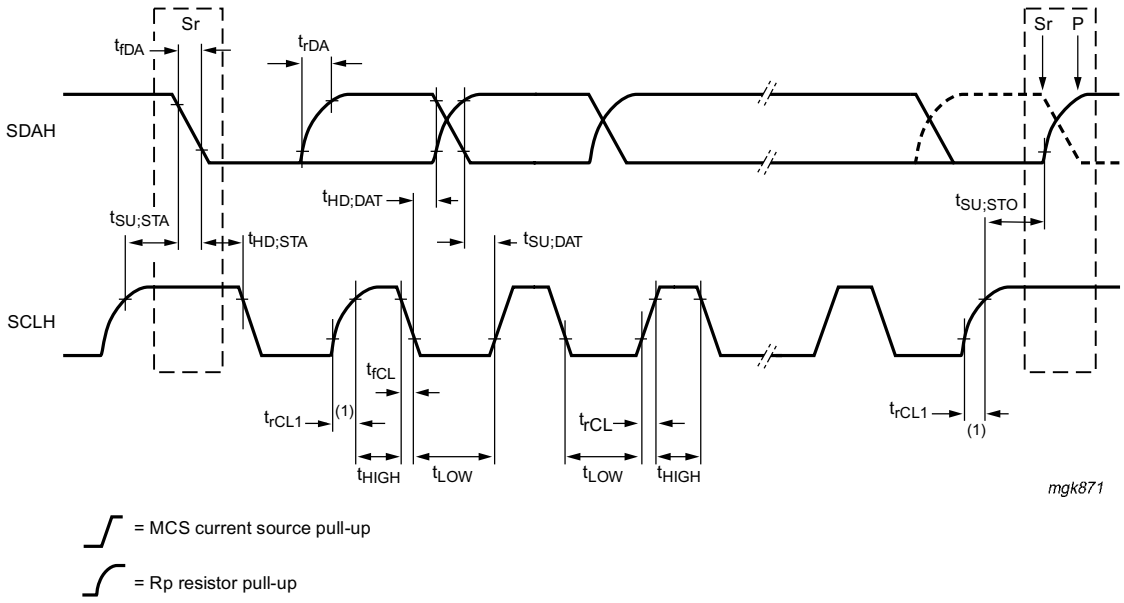


(1) First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Fig 28. Definition of timing for Hs-mode devices on the I²C-bus

7. Electrical connections of I²C-bus devices to the bus lines

7.1 Pull-up resistor sizing

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time. Figure 29 shows $R_{p(max)}$ as a function of bus capacitance.

Consider the V_{DD} related input threshold of $V_{IH} = 0.7V_{DD}$ and $V_{IL} = 0.3V_{DD}$ for the purposes of RC time constant calculation. Then $V(t) = V_{DD}(1 - e^{-t/RC})$, where t is the time since the charging started and RC is the time constant.

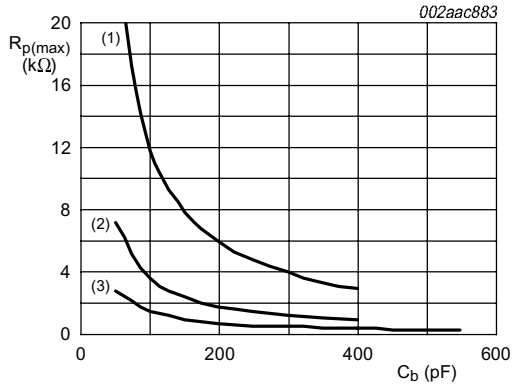
$V(t1) = 0.3 \times V_{DD} = V_{DD}(1 - e^{-t1/RC})$; then $t1 = 0.3566749 \quad RC$

$V(t2) = 0.7 \times V_{DD} = V_{DD}(1 - e^{-t2/RC})$; then $t2 = 1.2039729 \times RC$

$T = t2 - t1 = 0.8473 \times RC$

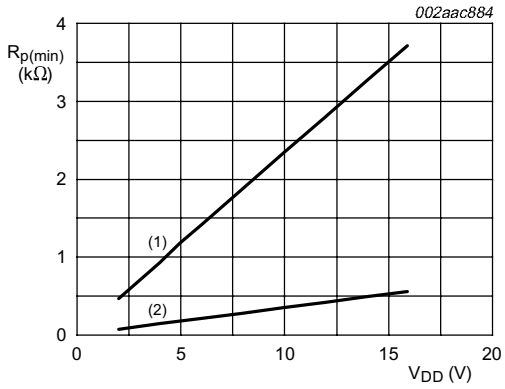
Figure 29 and Equation 1 shows maximum R_p as a function of bus capacitance for Standard-, Fast- and Fast-mode Plus. For each mode, the $R_{p(max)}$ is a function of the rise time minimum (t_r) from Table 6 and the estimated bus capacitance (C_b):

$$R_{p(max)} = \frac{t_r}{0.8473 \quad C_b} \tag{1}$$



(1) Standard-mode
(2) Fast-mode
(3) Fast-mode Plus

Fig 29. $R_{p(max)}$ as a function of bus capacitance



(1) Fast-mode and Standard-mode
(2) Fast-mode Plus

Fig 30. $R_{p(min)}$ as a function of V_{DD}

The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA for Standard-mode and Fast-mode, or 20 mA for Fast-mode Plus. $R_{p(min)}$ as a function of V_{DD} is shown in Figure 30. The traces are calculated using Equation 2:

$$R_{p(min)} = \frac{V_{DD} - V_{OL}}{I_{OL}} \quad (2)$$

The designer now has the minimum and maximum value of R_p that is required to meet the timing specification. Portable designs with sensitivity to supply current consumption can use a value toward the higher end of the range in order to limit I_{DD}.

7.2 Operating above the maximum allowable bus capacitance

Bus capacitance limit is specified to limit rise time reductions and allow operating at the rated frequency. While the majority of designs can easily stay within this limit, some applications may exceed it. There are several strategies available to system designers to cope with excess bus capacitance.

- Reduced f_{SCL} (Section 7.2.1): The bus may be operated at a lower speed (lower f_{SCL}).
- Higher drive outputs (Section 7.2.2): Devices with higher drive current such as those rated for Fast-mode Plus can be used (PCA96xx).
- Bus buffers (Section 7.2.3): There are a number of bus buffer devices available that can divide the bus into segments so that each segment has a capacitance below the allowable limit, such as the PCA9517 bus buffer or the PCA9546A switch.
- Switched pull-up circuit (Section 7.2.4): A switched pull-up circuit can be used to accelerate rising edges by switching a low value pull-up alternately in and out when needed.