

## **Logic Level MOSFET or Transistor Interfacing?**

Using logic level MOSFETs  
for interfacing your microcontroller to external devices.

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## Resources



### PIC C Course

A Complete C course for PIC micros in 11 parts.

CLICK the image.

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### PIC Interrupt Secrets

How to Use PIC Interrupts to Maximum effect.

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### State Machine Secrets.

How to use state machines to create **Solutions** to complex problems including fully debugged examples – one is coding a scrolling menu on a standard LCD display.

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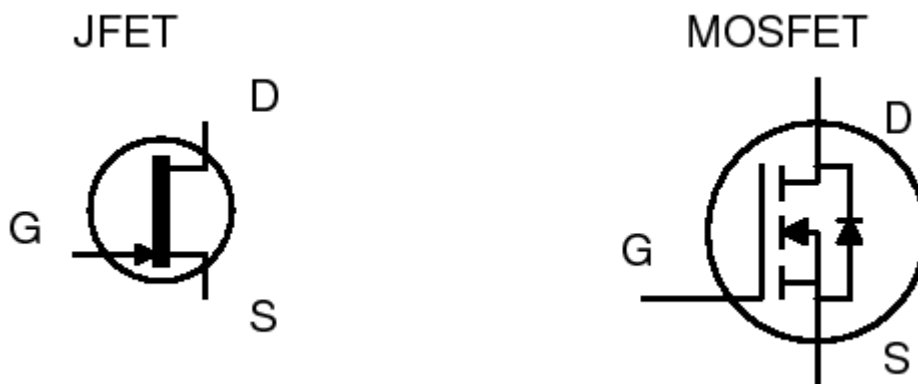
## Logic Level MOSFET or Transistor For Interfacing?

A logic level MOSFET may be easier.

If you are using transistors to interface to the outside world you may find FETs simpler, easier and better!

The traditional interfacing 'standard component' has always been the transistor. In fact I use these all the time on the bench but have you considered using a FET switch instead?

There are now so called "logic FETs" switch are ideal for 5V operation because the threshold point is designed to be around the 1V to 2V mark making them useful even for 3V systems as well.



Advantages of FETs:

- Can be driven by **logic** signals (if you use the right one i.e. a logic level MOSFET)
- Ability to drive **heavy loads** with very small power loss (unlike transistor)
- **Zero (near) input current** - there's no current needed from the uC pin.

You can't beat a FET when you want to control large loads e.g. motor driving - The low  $R_{ds}$  means that self heating is extremely low. This is unlike a transistor where the voltage across the transistor in saturation  $V_{ce}$  multiplied by the current flow means you burn your hand on the case! FETs are totally cool (pun intended).

Traditionally teaching is centered around the **bipolar transistor** because it was invented first because the **FET** process was more difficult even though it is the logical next step from a **valve**. The transistor is also easier in a way because

there is only one type not three and there are many standard circuit design blocks to choose.

Field Effect Transistors work as the name suggests by reacting to an electric field and not by using an electric current (as a transistor does). Since only the voltage is important there is no input current used it means that the **input impedance** of a FET is **extremely high** ( $Z=V/I$ ) and is only lowered by leakage current. So FET circuits with ultra high impedance input (many Giga Ohms) are easy and that's why they are used extensively in RF applications especially at the front end.

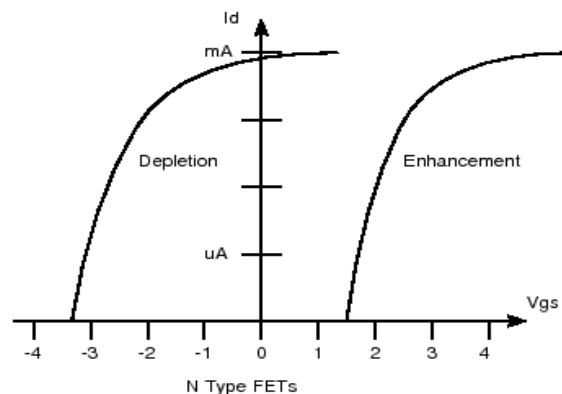
In fact a **FET** is easier to use than a transistor because it is **inherently stable** unlike the transistor which exhibits thermal runaway (it's why you need more resistors to provide negative feedback around an transistor amplifier to stop this effect).

The problem with **FETs** is that there are **three types** and they seem tricky to use mainly because they operate in slightly different ways whereas transistors are constructed in only one way i.e.NPN. N-type silicon, P-type silicon & N-type silicon (and of course the inverse PNP).

The three basic FET configurations are:

- JFET
- depletion mode MOSFET
- enhanced mode MOSFET

This I-V diagram shows the operation of the FET showing the current flow from Drain to Source  $I_d$  against the control voltage  $V_{gs}$  applied to the gate node.



*For a Logic Level MOSFET you need the right hand I-V curve.*

*Note JFETS are Depletion mode devices and  $V_{gs}$  must not go above zero volts (+0.5) otherwise due to construction a diode activates and current flows i.e. it does not behave as a FET anymer.*

In all cases the drain source and gate are analogous to emitter collector and base respectively.

| Transistor | FET    |
|------------|--------|
| Collector  | Drain  |
| Base       | Gate   |
| Emitter    | Source |

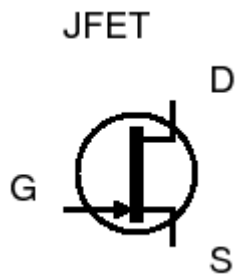
For an N FET the Drain is usually operated more positive than the Source (in the same way that the Collector is operated more positive than the Emitter in a transistor NPN design).

## FET Symmetry

Although FETs are designed with one terminal as the Drain and one as the Source (the drain usually has less capacitance for better output performance) it is true that either terminal can be the Drain or the Source because FETs are symmetrical.

In a FET either node can be the Source and the only definition is that the node with the lowest voltage (D or S nodes) is the source. To control the FET the  $V_{gs}$  gate voltage is always referenced to the source (the lowest voltage on the FET terminals D or S).

## JFET



For a JFET the gate is diffused directly into the silicon channel and the voltage at this gate controls the current flow from Drain to Source.

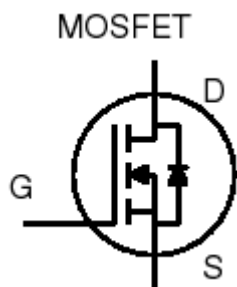
In general FETs are more useful for voltage systems where you have access to larger supply voltages ( $\pm 12V$  etc.) because you often have to take gate negative by up to 10 volts to fully turn off a JFET for instance (the exact voltage depends on the device construction and can vary with wide tolerance even for the same class of device).

*Note: Don't take the gate more than 0.5V above Source because it will turn into forward conducting diode!*

*Note: Drain and source are symmetrical in a FET so you can swap them! - but gate drain capacitance is designed to be less so it's usually used as the output i.e. less capacitance to drive means higher speed. You can tell which is the source node only by the voltages present i.e. source node is the node with the lower voltage on it!*

The big difference between a JFET and a NPN Transistor is that holding the gate voltage zero DOES NOT TURN IT OFF - you must hold the gate voltage negative compared to the source e.g. at -10V (depletion mode). This is the pinch off voltage or threshold voltage and it's why JFETs are not much use in logic systems. They are good for analogue switches and other analogue or RF designs. One standard well known device is the 2N3819.

## MOSFET



This is also known as an IGFET or Insulated Gate FET. The difference between the IGFET/MOSFET and the JFET is that there is an insulation layer between the Gate and the Drain/Source channel (shown in circuit symbol to left) i.e. the Gate is Insulated using Silicon Metal Oxide hence IG and MOS (Metal Oxide Silicon).

This is also why the MOSFET looks more complicated than the JFET or Transistor.

In addition to this there is always a parasitic diode present on the MOSFET which is often left out but should always be drawn. The parasitic diode arises as an unavoidable consequence in the way that the MOSFET is constructed. It is left out because in most cases it has no effect but it is important to know that it is present.

For example if you use a logic level MOSFET in a low current system where it's essential to save power the parasitic diode reverse current may be significant to the overall current budget of the design. It's doubly important in these systems as without drawing it you could think that there would be zero current flow when the MOSFET is off. In fact you could have a reverse parasitic diode current of a micro Amp. It doesn't sound a lot but in a critical low power circuit it may be



significant. Note: There is a way around it - and that is to use MOSFETs back to back - it works because of the symmetry of a FET.

## **MOSFETS (covers the logic level MOSFET)**

There are two types of MOSFET depletion and enhancement and they use the same symbols - the only difference is the position of the IV curve.

### **Depletion Mode MOSFET**

The depletion mode MOSFET has a similar characteristic to the JFET and again can only be turned off when the gate is held negative with respect to the source. So again it's not much use for LOGIC work.

### **Enhancement Mode MOSFET**

This is the logic level MOSFET i.e. it is the one to use and it has a characteristic curve where zero volts at the gate ( $V_{gs}$ ) turns off the output (Drain to Source current) and increasing the gate voltage progressively turns on the MOSFET i.e. it works in a similar way to the emitter follower where  $V_b$  held at zero turns off the collector current.

*Note: This is different operation to a transistor and you have to supply enough gate voltage to ensure that the correct current flows i.e. that the channel resistance is reduced enough.*

As mentioned logic level MOSFETs are FETs with a threshold voltage ( $V_T$ ) of about 1-2V (see the data sheet) and these will work directly with TTL or CMOS logic. The advantage you get is that they draw zero gate current.

A typical logic FET is the 2N7000 (low current 100mA) and another is the STP36NF06L (high current 30A) - You can find others in the catalogues.

## Transistor MOSFET Comparison

| Comparison of Logic Level MOSFET and transistor.                                                                                                                                                                                             |                                                                                                  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|
| Enhancement Mode MOSFET                                                                                                                                                                                                                      | Transistor                                                                                       |
| Ultra high input impedance (Z) gives zero i/p current.                                                                                                                                                                                       | Must supply current from driving pin - low input impedance (Z).                                  |
| Minimal external components.                                                                                                                                                                                                                 | Needs base resistor (to stop current saturation).                                                |
| Inherently stable (as amplifier).                                                                                                                                                                                                            | Inherently unstable (as amplifier)<br>Thermal runaway.<br>Ok for use as a common emitter switch. |
| Better logic level trigger point (2V typ) (less noise sensitivity).                                                                                                                                                                          | Only works at Vbe point (0.5V).                                                                  |
| Easy to blow up with static.                                                                                                                                                                                                                 | Difficult to blow up with static.                                                                |
| Very useful for driving high power (large I loads).                                                                                                                                                                                          | Not good at high power - generates heat and needs base current.                                  |
| Not good at RF speed because of inherent capacitance. Used only because of high i/p Z. More of a problem when driving high current which is why typical RF circuits use a FET at the front (High Z) followed by a transistor (High current). | Works well at RF.                                                                                |

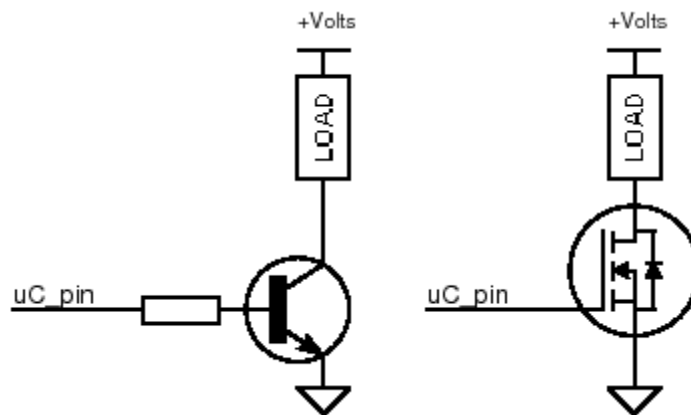
Probably the biggest problem is the device's sensitivity to static (the oxide layer is damage in a static event). If you interface the Drain or Source to outside pins then you need to ensure there is a static protection circuit in place to prevent damage.

## MOSFET and Transistor Drive circuits

Here's the equivalent circuits for transistor and MOSFET to drive loads that can be supplied from voltage sources higher than 5V:

**(Remember the current into the base of the transistor must be large enough to allow current through the load whereas for the FET you don't need any current drive at all – OK you do need some but it's so small  $\sim$ nA it is virtually zero).**

### Comparison of transistor and logic level MOSFET switching circuits



(Transistor on left, logic level MOSFET on right)

## FET High Z Control Warning

If you turn the microcontroller pin into an input the pin will be floating. FETs have extremely low input current requirement i.e. their input resistance is huge (Giga Ohms) and that means that any noise voltage from by nearby signals (or even other signals within the microcontroller will be coupled onto that input.

That means a voltage will appear on gate of the FET and if it becomes large enough it will turn the FET on.

*Note: This could also be a problem for critical circuitry at power up where most microcontrollers hold their pins as inputs i.e. safe until configured internally. There are some chips available that ensure fail safe operation (probably expensive) IC-MFN from [www.ichaus.de](http://www.ichaus.de)*

So you will have random operation of the system!

One way round it is to put a high value resistance from the gate to ground e.g. A 1M Ohm resistor. This leaks any induced charge at the gate away from the gate directly to ground, keeping the gate at zero volts i.e. the FET is always off. Also it does not interfere with the normal output operation of the microcontroller because it is such a high value.

Note: Transistors do not have this problem because they require high current (compared to a FET) in order to turn them on i.e. they have low input impedance at the base.