The Shift Register Model - SHIFTREG_#1

The SHIFTREG primitive model implements the functionality of a parallel/serial-in parallel/serial-out shift register. The model features:

- Shift up/down control via a CLK input and the shift direction control UP input.
- Register initialisation via the INIT property.
- Loading of the register's Q outputs from the D data inputs via the LOAD input pin. A synchronous or asynchronous load operation is definable via the ALOAD property.
- Resetting of the register's Q outputs via the RESET input pin. Synchronous or asynchronous reset is definable via the ARESET property.
- Shift enable/disable control via the HOLD input pin.
- Output-enable control via the OE input pin.
- Serial data inputs, DL and DU. When a shift up operation occurs, the less significant bits are moved one place up into the next more significant bit and the least-significant bit is loaded from the DL input. When a shift down operation occurs, the more significant bits are moved one place down into the next less significant bit and the most-significant bit is loaded from the DU input.

Serial data outputs, QL and QU. The QL output is the same as the least significant bit of the parallel output data, the QU output is the same as the most significant bit of the parallel output data. Unlike the parallel data outputs, the QL and QU are not affected by the OE output-enable input and remain active whilst the parallel outputs are tristate.

The OE output-enable input only affects the output state of the model's parallel data output. The OE input does not have to be asserted to perform reset, load or shift operations, and does not affect the output states of the QU and QL outputs.

In the case of more than one function being selected simultaneously, the reset operation has the highest priority, followed by the parallel load operation; given no reset or load operation and the HOLD input not being asserted, a shift operation will be performed in the direction indicated by the UP shift direction input.

Pin	Type	Pin Set	Description
CLK	Input	-	Clock
RESET	Input	-	Data Reset
LOAD	Input	-	Data load
HOLD	Input	-	Shift-hold
UP	Input	-	Direction control
DL	Input	-	New lower data
DU	Input	-	New upper data
D#	Input	#1	Parallel load data
Q#	Output	#1	Data output
QL	Output	-	Lower Q output
QU	Output	-	Upper Q output

Time	Type	From/To	Edge	Default	Notes
TDLHCQ	Delay	CLK → Q	L → H	0	
TDHLCQ	Delay	CLK → Q	H → L	0	
TDLHLQ	Delay	LOAD →	L → H	TDLHCQ	[1]

		Q			
TDHLLQ	Delay	LOAD → Q	H → L	TDHLCQ	[1]
TDHLDQ	Delay	D# → Q	H → L	TDHLCQ	[1]
TDLHDQ	Delay	D# → Q	L → H	TDLHCQ	[1]
TDLZOQ	Delay	OE → Q	L → Z	TDLHCQ	
TDHZOQ	Delay	OE → Q	H → Z	TDHLCQ	
TDZLOQD	Delay	OE → Q	Z → L	TDHLCQ	
TDZHOQ	Delay	OE → Q	Z → H	TDLHCQ	
TDRQ	Delay	RESET → Q	H → L	TDHLCQ	
TGQ	Glitch	ANY → Q	Pulse	TDxxCQ	

Property	Type	Meaning	Default
INIT	Initialisation	Initial register contents	0
ARESET	Boolean	Asynchronous RESET?	FALSE
ALOAD	Boolean	Asynchronous LOAD?	FALSE

1. The LOAD to Q time is used on LOAD going active (with a clock edge for a synchronous load); the D to Q time is used for a change in the input data whilst LOAD is already active.